NPTEL-Phase-II : Course : Advanced VLSI Design

Question Set for Module 5 and Module 6 : prepared by Dr. Sachin B. Patkar (Professor, Dept. EE, IIT Bombay)

 Module 5:
 FSM Controller/Datapath and Processor Design

 Textbook :
 [WH book] "*CMOS VLSI Design* " by Neil H. E. Weste, David F. Harris , Pearson

 [PH book] "Computer   Organization and Design, Fourth Edition: The Hardware/Software Interface ", David A. Patterson, John L. Hennessy, Morgan Kaufmann, 2008

 Module 6:
 VLSI Design Automation

 Textbook : [KLMH book] **"**VLSI Physical Design: From Graph Partitioning to Timing Closure", by Kahng, Lienig, Hu and Markov,   Springer, 2011

Checkpoint Questions :

Question :
 What is meant by (single-clock-edge-triggered) synchronous sequential logic circuit ?

Question :
 Explain the vocabulary : rising edge, falling edge, edge-triggered memory element, clock cycle, extent of a clock cycle in a falling edge triggered sequential logic circuit.

Question :
 What is the main advantage of synchronous sequential logic design over asynchronous one ?

Question :
 What are the setup and hold requirements of an edge-triggered memory element ?

Question :
 What is meant by a "value" of an input signal during a particular clock cycle ? Clearly the signal value is not always stable, therefore there needs to be some clarity on what is meant by the "value" of an input signal during a specified clock cycle.

Question :
 What is a datapath ? What is an FSM ?

Question :

What are the typical components of a datapath ? Why are they regarded as components of a datapath ?

Question :
What is difference between custom computing machine and a general purpose computing machine ?

Question :
If a datapath component for computing a remainder were available, what would have been the major simplification to the GCD (custom) computing machine.

Question :
What is the task of the FSM part of a computing machine that has been designed using the architecture style known as FSM+datapath ?

Question :
What are the inputs and the outputs of the FSM used in the design of the GCD computing machine ?

Question :
Where do the output signals, of the controlling FSM in the example of GCD computing machine, go ?

Question :
What are the states of the controlling FSM of the GCD computing machine ?

Question :
What are the datapath components used in the datapath of the "GCD" computing machine ?

Question :
What typical part of Verilog HDL code describes a multiplexer in a natural way.

Question :
What is trivial about a single state FSM ?

Question :
What was the benefit achieved by enhancing the single state FSM for GCD computing to FSM that contains states stIDLE and stLOOP ?

Question :
Express in your own words, how the state diagram is routinely translated into corresponding Verilog HDL code fragment.

Question :
What are the input signals needed by the FSM part of the custom computing machine for binary multiplication that was described in a lecture in this module.

Question :

Enumerate the control signals generated by the FSM part of the custom computing machine for binary multiplication that was described in a lecture in this module.

Question :

What are the datapath components used in the datapath of the "binary multiplication" computing machine ? Which of them are purely combinational and which of them have the ability to remember the data across clock cycles ?

Question :

What are the states of the FSM part of the custom computing machine for binary multiplication that was described in a lecture in this module ?

Question :

What does RISC stand for ?

Question :

What are the datapath components of the single-cycle microarchitecture for mMIPS ?

Question :

What are the control signals generated by the controller part of the single-cycle microarchitecture for mMIPS ?

Question :

What are the datapath components of the multi-cycle microarchitecture for mMIPS ?

Question :

What are the control signals generated by the controller part of the multi-cycle microarchitecture for mMIPS ?

Question :

What is the main motivation behind the multi-cycle microarchitecture for mMIPS, although a single-cycle mMIPS would certainly have been able to perform any computation that can be carried out by the multi-cycle version ?

Question :

Why is the "computing ability" invariant of whether we use a single-cycle or a multi-cycle microarchitecture for mMIPS ?

Question :

Is the "computing speed" too invariant of the microarchitecture chosen to implement the ISA of mMIPS ?

Question :

What are the overheads of a multi-cycle microarchitecture in comparison with a single-cycle microarchitecture ? On the other hand what resource requirement might be reduced in a multi-cycle uArchitecture ?

Long Answer Questions

Question :

Trace through the execution of the GCD FSM+datapath for the input pair 84 and 102

Question :

Design a ones-counting circuit (that counts the number of 1's in an 8-bit input to the datapath). The datapath should use a shift register and a counter along with other necessary components. Describe the FSM and the datapath for this task.

Question :

Add to the single-cycle micrcoarchitecture of mMIPS, the "swap" instruction, which exchanges the contents of two MIPS registers, for example,

swap $5, $6

swaps the contents of the registers 5 and 6.

Question :

Add to the multicycle micrcoarchitecture of mMIPS, the "swap" instruction, which exchanges the contents of two MIPS registers, for example,
swap $5, $6
swaps the contents of the registers 5 and 6.

Question   : (from [KLMH book])
Let G(V,E), where V={a,b,c,d,e,f} and E={(a,d), (a,e), (b,e), (b,f), (c,f), (b,c), (d,e), (e,f)} be the given graph to be partitioned using Kernighan-Lin's algorithm. Assume that the initial partition is taken as { (a,b,c), {d,e,f} }. Trace the execution of the passes of K-L algorithm on this example.
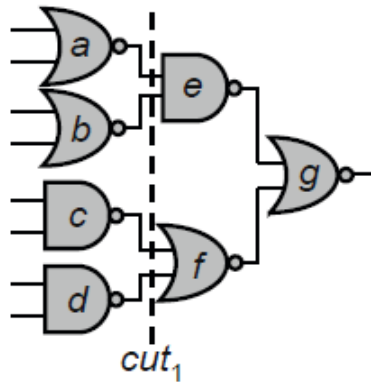
Question :

Perform min-cut placement to place gates a-f, that are interconnected in pairs as {(a,d), (a,e), (b,e), (b,f), (c,f), (b,c), (d,e), (e,f)}, on a 2 × 4 grid. Use the Kernighan-Lin algorithm for partitioning.

Use alternating (horizontal and vertical) cutlines.

Question : (from [KLMH book])

Min-Cut Placement : Perform min-cut placement to place gates a-g on a 2 × 4 grid. Use the Kernighan-Lin algorithm for partitioning. Use alternating (horizontal and vertical) cutlines. The cutline cut_1 represents the initial vertical cut.

cut_1

Question :

Assume that in the given implementation technology 2-input AND and 2-input OR gates exhibit a delay of 2 time units each. The inverter delay is 1 unit. Suppose these are the only types of gates available for implementation. What is the best (**best** as far as the longest combinational path delay is concerned) implementation of a 8 input odd-parity circuit which outputs 1 if and only if odd number of inputs among the 8 inputs are HIGH. Trace the execution of the static timing analysis algorithm, assuming that the required arrival time at the output is 15.

Question :

Prove that the left edge algorithm uses minimum number of horizontal tracks (assuming that no two pins are on the same vertical line).

Question : (from [KLMH book])

Given the logic circuit below, draw the timing graph (a), and determine the (b) AAT, (c) RAT, and (d) slack of each node. The AATs of the inputs are in angular brackets, the delays are in parentheses, and the RAT of the output is in square brackets.